13. (Amended) A system for synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, comprising:

means for determining if there is any difference between the local and program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock values, or an absolute difference between the local clock value and the program value, so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.

REMARKS

Claims 1-10 and 13-15 are pending in this application. In the Office Action, the Examiner rejected Claims 1-5 and 13-15 under 35 U.S.C. §112, second paragraph, as being indefinite, and the Examiner rejected Claim 6 under 35 U.S.C. §102 as being fully anticipated by the Mills paper "RFC 1305 Network time Protocol (Version 3)." The Examiner also objected to the specification, and in particular, to page 4, lines 7-15. Claims 7-10 were allowed, and none of claims 1-5 or 13-15 was rejected over the prior art.

Claims 1, 3 and 13 are herein being amended to improve the form and readability of the claims. Also, Claim 6 is being cancelled, and the specification is being amended to overcome the Examiner's objection.

More specifically, page 4 of the specification is being amended to delete the redundant phrase occurring in the sentence on lines 7-15. In view of this, the Examiner is requested to reconsider and to withdraw the objection to the disclosure.

Also, it may be noted, because Claim 6 has been cancelled, this claim is no longer an issue.

With respect to the rejection of Claims 1-5 and 13-15 under 35 U.S.C. §112, the preambles of independent Claims 1, 3 and 13 are being amended to provide express support for the limitations "program clock" and "program clock frequency." Specifically, the preambles of Claims 1 and 3 are being amended to describe "A method of synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock," and this provides the support for references to the program clock and to the program clock frequency occurring later in these claims and in subsequent claims. Analogously, the preamble of Claim 13 is being amended to describe "A system for synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock," and this provides support for references to the program clock frequency later in this claim.

Also, Claim 3 –specifically, the step beginning "if there is a difference"- is being amended to include the limitations of original claim 1 that were inadvertently not added to this step of Claim 3 in Applicant's previous Amendment.

Attached hereto is a marked-up version of the changes made to the specificatin and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

With these changes to Claims 1, 3 and 13, all of Claims 1-5 and 13-15 are clear and definite and fully comply with the requirements of 35 U.S.C. §112. The Examiner is, accordingly, respectfully requested to reconsider and to withdraw the rejection of these Claims as being indefinite.

Applicant respectfully submits that this Amendment places the entire application in condition for allowance. In particular, the Examiner is respectfully requested to reconsider and to withdraw the objection to the disclosure and the rejection of Claims 1-5 and 13-15 under 35 U.S.C. §112, and to allow these Claims. If the Examiner believes that a telephone conference with Applicant's Attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,

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"VERISON WITH MARKINGS TO SHOW CHANGES MADE"

IN THE SPECIFICATION:

Replace the paragraph on Page 4, lines 6-28 with the following:

The MPEG-2 System Layer has the basic task of facilitating and multiplexing of one or more programs made up of related audio and video bitstreams [of one or more programs made up of related audio and video bitstreams] into a single bitstream for transmission through a transmission medium, and thereafter to facilitate the demultiplexing of the single bitstream into separate audio and video program bitstream for decompression while maintaining synchronization. By a "Program" is meant a set of audio and video bitstreams having a common time base and intended to be presented simultaneously. To accomplish this, the System Layer defines the data stream syntax that provides for timing control and the synchronization and interleaving of the video and audio bitstream. The system layer provides capability for (1) video and audio synchronization, (2) stream multiplex, (3) packet and stream identification, (4) error detection, (5) buffer management, (6) random access program insertion, (7) provide data, (8) conditional access, and (9) interoperability with other networks, such as those using asynchronous transfer mode (ATM).

IN THE CLAIMS:

Cancel Claim 6.

Amend Claims 1, 3 and 13 as set forth below.

1. (Thrice Amended) A method of [adjusting] synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the decoder includes

hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, the method comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

including the steps of:

i) using the hardware to adjust the local clock frequency until a threshold condition occurs, and

iii) after the threshold condition occurs, using the processor to adjust the local clock frequency.

3. (Twice Amended) A method of [adjusting] synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the local clock oscillates at a local clock frequency, the method [further] comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify the program clock value and frequency;

maintaining a program clock value based on the clock signals received at the decoder;

determining if there is any difference between the local clock and the program clock frequencies;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is either a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the processor to adjust the local clock frequency.

13. (Amended) A system for [adjusting] synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, comprising:

means for determining if there is any difference between the local and program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock values, or an absolute difference between the local clock value and the program value, so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.